LOW-POWER EMBEDDED VECTOR DSP

EVP VD32041 32-bit embedded-vector processor for SoCs

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The VD32041 DSP is a high-performance vector processor for applications with high computational load. Its low power consumption and small size make it an ideal building block for implementing multi-standard modems for 3G (HSPA/TD-SCDMA) and 4G (LTE FDD/TDD), WLAN (802.11n), MBMS, DVB/DAB, and comparable standards.

This area-efficient, low-power core brings a new level of programmability to complex application functionality used in OFDM and RAKE/CDMA based modems, making it easy to add differentiating features and keep pace with evolving standards.

KEY FEATURES

- Ultra high-performance, low-power embedded DSP core
- Advanced vector processing
  - SIMD operations
  - 256-bit vector width
  - Intra-vector operations such as segmented add and vector permutation
- Efficient scalar and address processing in parallel with vector processing
- VLIW instruction execution
  - 6 parallel vector operations
  - 4 parallel scalar operations
  - Up to 100 operations per cycle (16 bit)
- Full support for C control structures, including:
  - Zero overhead looping
  - Predicated operations
  - Stack frame support
- Up to 5 billion multiply-accumulate operations per second (clock running at 300 MHz)
- Code generator for scrambling and generating channelization codes
- AMBA™ AXI master interface for control
- AMBA™ AXI slave interface
- CoreSight™ prepared debug and trace infrastructure via AMBA APB and AMBA ATB interfaces

KEY BENEFITS

- Software defined modem instead of a collection of hardware accelerators
- Easy integration into SoC environment
  - Single-edge clock design
  - Technology-independent fully synthesizable design
  - Use of standardized interfaces
- Programmable in standard C with vector extensions
- High performance in complex vector algorithms
- Efficient mapping of regular and irregular algorithms

TARGETED APPLICATIONS

- Mobile phones
- Mobile data cards and dongles
- Multi-standard modems
- Femtocell base stations

CORE DETAILS

Operating at 300 MHz, the VD32041 is capable of running up to 30 GOPS (giga operations per second) on 16-bit data. This includes 5 billion multiply-accumulate operations per second.

By combining the versatile, general-purpose processor architecture with a fully C-based programming model, the VD32041 improves performance in complex algorithms. Being more than a SIMD (single instruction, multiple data) machine, the core provides highly-efficient mapping of regular and irregular algorithms. For example, a self-sorting, 64-point complex FFT kernel operates in 50 cycles.

The VD32041 features arbitrary shuffling of vector elements and intra-vector operations working on multiple elements within the same vector, such as permutations, multi-element additions, and min/max finding. Vector parallelism, along with a very long instruction word (VLIW) instruction concept, enable the VD32041 to operate on multiple vectors in parallel.

Strong scalar and decision-making capabilities enable the control code of an application to be mapped onto the processor, so it can operate independently from the host. Working on a frame basis, for example, the VD32041 significantly reduces inter-processor communication requirements.

LOW POWER, SMALL FOOTPRINT

The subsystem employs a single-edge clocking strategy that uses extensive power-saving measures.
In a low-power 45 nm process, the typical power consumption, including data and program memory, is less than 0.5 mW/MHz (typical application code mix). The DSP area, including a 4 K x 256 data memory and a 128-Kbyte program memory, is less than 3.2 mm^2.

SOC INTEGRATION

Designed for use as an IP block, the VD32041 core with surrounding subsystem (the layer containing memories and interfaces) are easy to integrate into a system-on-chip (SoC) design. It supports multi-processor architectures, and employs an industry-standard AMBA AXI bus interface.
The subsystem facilitates multi-core debugging via its CoreSight-prepared debug and trace infrastructure, which uses AMBA advanced peripheral bus (APB) and AMBA advanced trace bus (ATB) interfaces.

CORE ARCHITECTURE

The VD32041 core can be divided into four basic blocks: the program control unit, the vector data computation unit, the scalar data computation unit, and the address computation unit.

PROGRAM CONTROL UNIT (PCU)

The PCU uses VLIW encoding with a compression scheme that reduces code size. The open, visible pipeline results in a simple, power-efficient core that requires no interlocking or hardware dependency analysis logic.
The complexity of scheduling and dependencies is moved from hardware to the compiler.

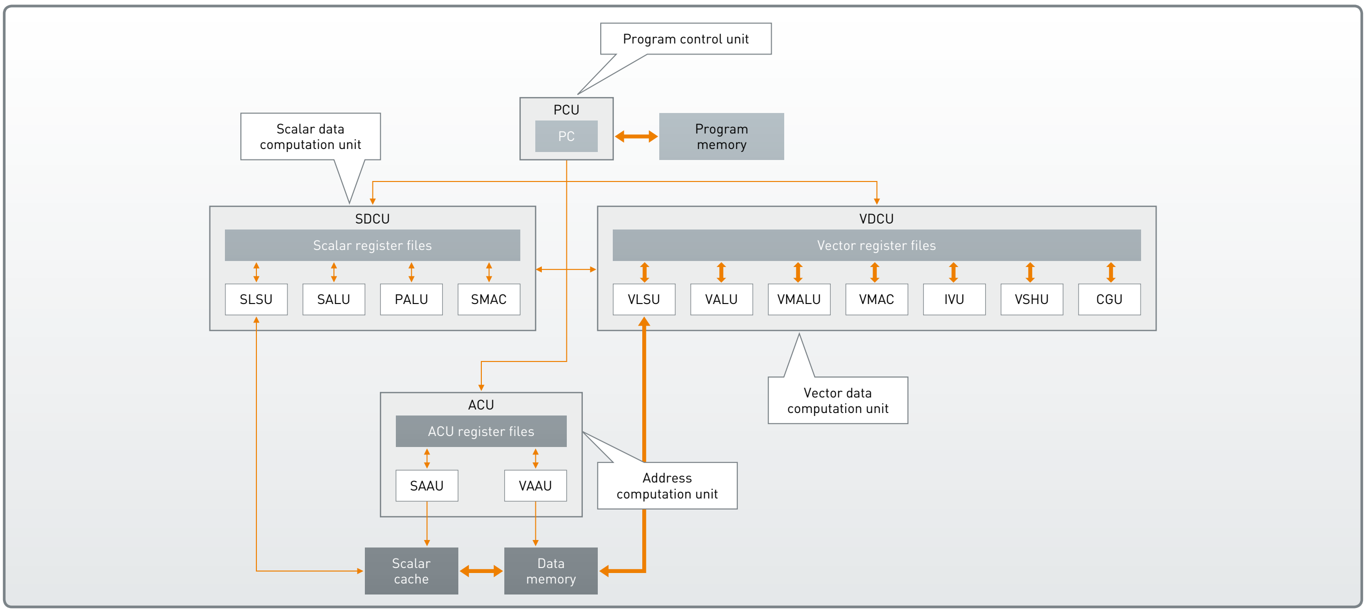
To support conditional branches and calls, the PCU can perform conditional execution via predicates, computed in the the scalar path. Also, most instructions can be predicated, to eliminate branching altogether for short if-statements, removing pipeline penalties. Zero-overhead looping further reduces pipeline impacts, allowing loops to run at full speed, not needing additional cycles for loop counter computations.

TYPICAL PERFORMANCE CHARACTERISTICS (45 nm CMOS LOW-POWER PROCESS)

Clock	0 to 320 MHz	
MAC operations per second	5 billion	
Active power consumption	< 0.5 mW/MHz (typ.)	
Area	Core logic	1.3 mm^2
	Core with typical memory configuration: 128-Kbyte program; 4 K x 256 data memory	3.2 mm^2

APPLICATIONS

Communications	3G (HSDPA/TD-SCDMA), 4G (LTE FDD/TDD), MBMS
Connectivity	WLAN (IEEE 802.11n), WiMAX
Broadcasting	TV-on-mobile, DVB-S/H/T, DAB



VD32041 functional diagram

VECTOR DATA COMPUTATION UNIT (VDCU)

The VDCU is the central vector processing kernel of the core. Operating on 256-bit vectors, it supports both SIMD and intravector-style computations with native support for integer, fixed-point and complex data types. All operations can be performed in masked mode, where a bitvector mask indicates active vector elements. The vector mask ALU (VMALU) enables bitwise logical operations on the vector mask registers.

The VDCU has two shared register files, a 16-entry vector register file and an 8-entry mask register file. Using the vector load store unit (VLSU), vector registers can be transferred to and from memory. Vector-aligned load-and-store operations, as well as unaligned vector loads, are supported.

The vector arithmetic logical unit (VALU) performs conventional SIMD-style arithmetic and logical operations, data-type conversions, barrel shift operations, and move operations. The unit also supports special functionality, including operation selection via the use of predicate registers, division, and conditional operations.

The intra vector unit (IVU), a non-SIMD unit, operates on the complete vector, supporting functions such as summing part of the vector and finding the min/max element within a set of vectors. The vector multiply/accumulate (VMAC) unit performs multiply and MAC operations in 16-, 32-, or 40-bit formats, with optional rounding and saturation. An extra adder/subtractor is included to offload the ALU when dealing with arithmetic-intense algorithms. Scramble and descramble functions are supported.
The vector shuffle unit (VSHU), another non-SIMD type unit, shuffles elements in a single vector by operating on a complete vector with a granularity of 8, 16, or 32 bits. The elements can be rotated, shifted, or copied within the vector or arbitrarily shuffled, by element, according to freely programmable patterns. Insertion and extraction of words in the vector are also possible.

The code generation unit (CGU) is an application-specific unit used to create scramble and channelization codes. It generates 16 sequential bits per cycle.

SCALAR DATA COMPUTATION UNIT (SDCU)

The SDCU operates on 8-, 16-, and 32-bit integer/fixed-point data and behaves as a 16/32-bit RISC CPU. Scalar results can be broadcast to the VDCU for use as vector input operands. Vice versa, a scalar can be selected from a vector register as input to the SDCU. There are two shared register files, the scalar register file with 32 general-purpose registers of 16 bits each, and the predicate register file with eight predicates of one bit each. Within the SDCU, the scalar load store unit (SLSU), scalar ALU (SALU), predicate ALU (PALU), and scalar MAC unit (SMAC) are available

ADDRESS COMPUTATION UNIT (ACU)

The ACU provides parallel memory access for the scalar and vector memories. The ACU contains four shared 32-bit register files, each with eight pointer registers, eight base registers for circular buffers (or use as extra pointers), eight size registers indicating the size of the buffer, and eight offset registers for offset addressing.

SOFTWARE DEVELOPMENT KIT

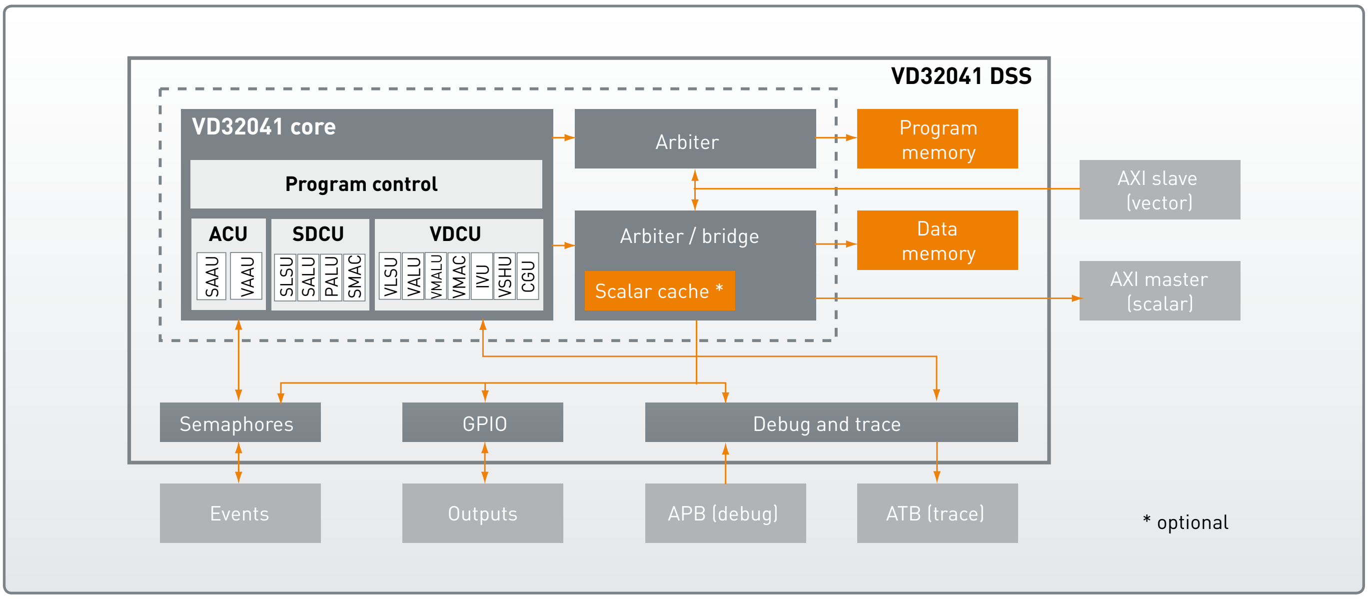
The VD32041 is accompanied by a software development kit (SDK), a complete design environment supporting multi-core SoC architectures and offering a full set of tool components plus documentation.

Programmers use the Eclipse-based integrated development environment (IDE) as the main interface to the design. The underlying tool chain includes an EVP-C compiler, assembler, linker, and a high-speed instruction set simulator. The package also includes other tools, such as a profiler and an emulator that can link to hardware such as test chips or FPGAs. The kit is also provided with a MatLab interface. For system-level simulation, a fast System-C model is available.

EVP-C increases programmer productivity by hiding many of the architectural details, such as pipeline latencies and register files. The vector and fixed-point data types are extensions to standard C. Since EVP-C is a subset of C++, programmers can start their design, expressing vector parallelism and exploiting EVP-specific data types as complex fixed-point data while using familiar tools such as C++ compilers and verification frameworks on a PC or workstation. Only after the new, more parallel code has been verified do programmers need to start working in the dedicated VD32041 tool chain.

FIRMWARE LIBRARIES

In order to speed up firmware development, a library of often-used modules is available. The library contains functions such as FFT, IFFT, FIR, square root, matrix arithmetic, normalization and Cordic functions. For each function, both a reference implementation and a test suite is delivered, allowing further tuning to application-specific needs.



VD32041 subsystem

LET'S CREATE IT

Order code: BRSTNDSP1208

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