3D Packaging

ISSUE N°19
MAY 2011

Magazine on 3DIC, TSV, WLP & Embedded die Technologies

FEATURE STORIES
Flip-chip & wafer bumping trends

COMPANY INSIGHT
ST-Ericsson wireless packaging roadmap update

WHAT'S INSIDE?
Visera silicon WLP of HB-LED module

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COMPANY VISION

ST-Ericsson wireless packaging roadmap

The pace of Innovation in packaging has probably never been faster than in recent years. Companies are continuously pushing technology to the limit to deliver leading-edge solutions while mobile devices are clearly at the forefront of many of these innovations.

Yann Guillou
3D & Advanced Packaging
BE Technology Sourcing
ST-Ericsson

The packaging solution for a product or a family of product is now decided at a very early stage of product definition and a tight co-design between the IC and the package is necessary to achieve optimal results. Performance, cost, miniaturization, integration, time to market are the key words driving all the latest packaging technologies.

ST-Ericsson is pioneering and implementing many of these technologies in its product portfolio to deliver best-in-class solutions to its customers. In the rest of this article, the focus will be on some key packaging technologies that ST-Ericsson is focused on for the future: Bumping & Flip Chip, Wafer Level Package, Next Generation PoP and Through Silicon Via.

Bumping & flip chip

Flip chip products are already widely used in mobile devices and will continue to be used for some time. I/O density and the increasing performance demands of mobile computing are mandating shorter paths between the individual ICs and PCB and traditional wires cannot satisfy all the requirements. Application processors were the 1st products to move from wires to bumps. Now, all the core components of the mobile platform chipset are going in this direction, including RF transceivers and power management ICs. In the future only a limited amount of ST-Ericsson new products will still be designed with wire bonding.

If we have a closer look at bumping, we see that solder bump is the mainstream technology down to 45nm CMOS while copper pillar technology is gaining traction. It is interesting to note the different approaches emerging, mainly between peripheral bumping with fine pitch versus a matrix approach with a more relaxed pitch. Each approach has pros and cons and their use can be application dependent. They will sometimes require the use of techniques such as mass reflow or thermo-compression associated with capillary or pre-applied underfill. Molded underfill is another option that can be considered in some specific cases.

"Fan Out WLP is suitable for larger packages and higher I/O count as is the case of the core chips of a wireless platform," explains Yann Guillou, ST-Ericsson.

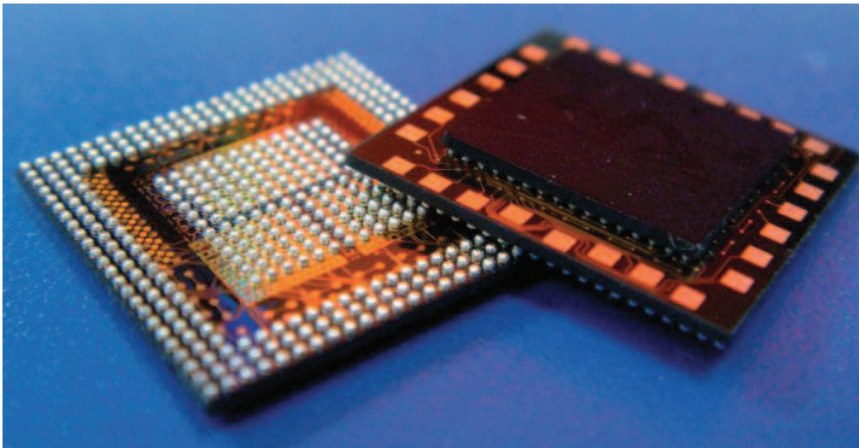
Wafer Level Chip Scale Package

Wafer Level Chip Scale Package (WLCSP) is a growing packaging option for mobile devices. It enables both great miniaturization and high performance. WLCSP can be divided into two categories, both of which are used by ST-Ericsson in its latest products: Fan-In Wafer Level Packaging (FIWLP) and Fan-Out Wafer Level Packaging (FOWLP). In both cases, no laminate substrate is needed to connect the die to the PCB. BGA balls are directly attached onto the silicon die and/or the fan out area. Fan-in WLP fits devices with small dies and relatively low I/O count such as connectivity combos and RF power management ICs. Fan Out WLP is suitable for larger packages and higher I/O count as is the case of the core chips of a wireless platform. Fan Out WLP is able to deliver maximum benefits when the silicon die and the package are tightly co-designed. As the technology is maturing and the option scope expands, the Fan Out WLP application space is widening and becoming more attractive.

Next generation PoP

PoP (Package on Package) for Digital BaseBand and Application Processors have been in ST-Ericsson products since the first 65nm digital products and this is planned to continue. However, new emerging PoP technologies need to be specifically developed to meet the evolving requirements. Package thickness needs to be drastically reduced, warpage has to be controlled, top package ball pitch needs to be reduced to allow more I/O between the processor and the memory, and thermal behavior need to be managed in a good way.

At the same time, CMOS technologies are becoming more and more brittle. As a result, some new wafer passivation, substrate core materials and substrate finishing are being developed. The PoP concept with laser drilled vias in the mold compound is one attractive way forward. The die in the bottom PoP package can be overmolded or exposed by using film assist techniques - the final goal being to find the best trade-off between the package thickness, warpage and cost of the solution. Alternatively, disruptive PoP concepts based on Fan Out WLP could emerge in mid term. Pilot products are under evaluations for future use and the results so far are encouraging.



Fan Out WLP PoP (Courtesy of STMicroelectronics, STATS Chip PAC and Infineon)

the initial plans agreed in JEDEC committee and complementary standardization initiatives have been running. Some items still need to be solved before the technology is truly ready for high volume manufacturing but progress is regularly made.

To turn this into a viable business there are still a number of things to be clarified in the supply chain and the ecosystem. Some of the main sticking points today are around ownership of middle end process, the test strategies and the business models that will exist between the actors.

Through Silicon Via (TSV)

Via middle TSV done between the Front End Of Line and Back End Of Line filled by copper in a foundry is also a technology ST-Ericsson is considering for future products. While still at early investigation stages 2 or 3 years ago, the wireless industry clearly found one of its driving products to focus the TSV developments for some time now. Technology options have been drastically screened down driven by the application requirements of what is called the wide I/O interface.

Wide I/O is being embraced by the industry and is identified as a promising solution to deliver the best bandwidth/power consumption ratio for data transfer between a low power processor and DRAM memories.

Much has been done by foundries to develop technology platforms that include TSV option. Packaging houses have accelerated their equipment investments to install and qualify the missing 300mm tools. Memory providers have also progressed in line with

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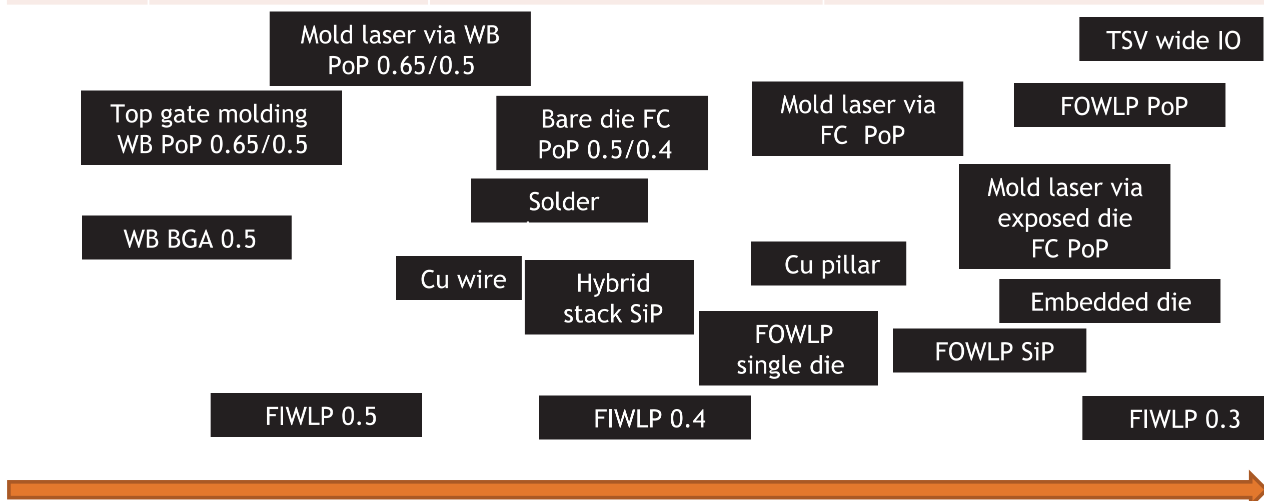
Yann Guillou leads 3D and advanced packaging in the CTO and Strategic Planning Office at STEricsson. Guillou began his career at CEA-LETI and then worked at STMicroelectronics and ST-NXP.
He holds a MSc. in materials and nanotechnology from the National Institute of Applied Sciences, and a Masters in Management of Technology and Innovation from Grenoble Business School, France.

ST-ERICSSON PACKAGING INNOVATION

Year	2008	2010	2012 +
CMOS	>65	45nm	<32nm
Interco	WB	WB & FC solder	FC solder and Cu pillar
Techno	BGA	BGA, WLCSP	BGA, WLCSP, TSV
Pitch	0.5mm	0.4mm	0.4mm (incl. PoP top)



(Courtesy of ST-Ericsson)